



CWD LIMITED

Datasheet

CBTLRM01

Multiprotocol ANT, 2.4GHz, LoRaWAN

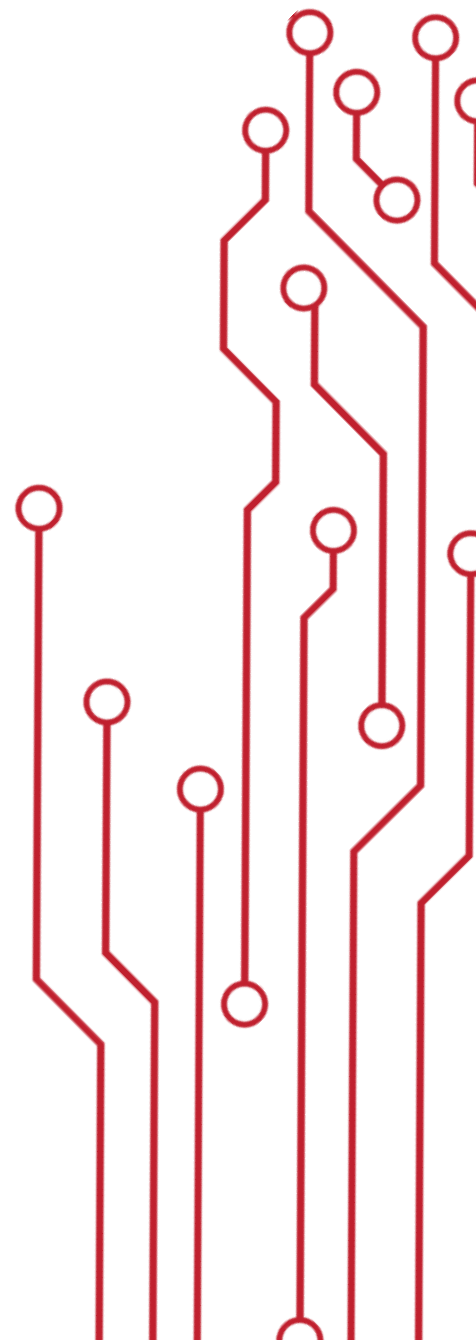


Table of Contents

1. General Description	3
2. Applications	4
3. Features.....	6
4. Application Block Diagram.....	10
5. Interfaces.....	11
5.1. Power Supply	11
5.2. System Function Interfaces	11
5.2.1. GPIOs.....	11
5.2.2. Two-wire Interface (I2C Compatible).....	12
5.2.3. Flash Program I/Os.....	12
5.2.4. SPI Bus.....	12
5.2.5. UARTs	13
5.2.6. Analogue to Digital Converter (ADC)	13
5.2.7. Low Power Comparator (LPCOMP).....	14
5.2.8. Reset	14
5.2.9. NFC.....	14
6. Module Specifications.....	16
7. Module Pin-out and Pin Description.....	17
7.1. Module Pin-out	17
7.2. Pin Description.....	18
8. PCB Footprint and Dimensions	20
9. Electrical Characteristics	21
9.1. Absolute Maximum Ratings	21
9.2. Recommended Operating Range	21
10. Ordering Information.....	22
11. Contact Information	22

1. General Description

The CBTLRM01 (2.4GHz+LoRa) module is a multiprotocol highly flexible, ultra-low power module that supports 2.4GHz and LoRaWAN™ using Nordic nRF52832 and Semtech's SX1262 SoC solutions developed by CWD Limited.

The module is designed for high data rate long-range wireless communication in the 2.4GHz ISM band and 150 MHz to 960 MHz bands for LoRa. Further the module supports, ANT protocol and LoRaWAN® standard for proprietary protocols. The module can transmit up to +22 dBm with highly efficient integrated power amplifiers on LoRa and can transmit up to +4dbm in 2.4GHz.

2. Applications

Due to varied support of protocols and stacks, the CBTLRM01 module can support varied applications. A brief of the applications is as below:

LoRa	<ul style="list-style-type: none"> • Smart meters • Supply chain and logistics • Building automation • Agricultural sensors • Smart cities • Retail store sensors • Asset tracking • Streetlights • Parking sensors • Environmental sensors • Healthcare • Safety and security sensors
2.4GHz	<ul style="list-style-type: none"> • Internet of Things (IoT): <ul style="list-style-type: none"> ▪ Home automation ▪ Sensor networks ▪ Building automation ▪ Industrial ▪ Retail • Personal area networks: <ul style="list-style-type: none"> ▪ Health/fitness sensor and monitor device ▪ Medical device

	<ul style="list-style-type: none">▪ Key fobs and wrist watches• Interactive entertainment devices:<ul style="list-style-type: none">▪ Remote control devices▪ Gaming control• Beacons• A4WP wireless charger and devices• Computer peripherals and I/O devices:<ul style="list-style-type: none">▪ Mouse▪ Keyboard▪ Multi-touch trackpad▪ Gaming
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3. Features

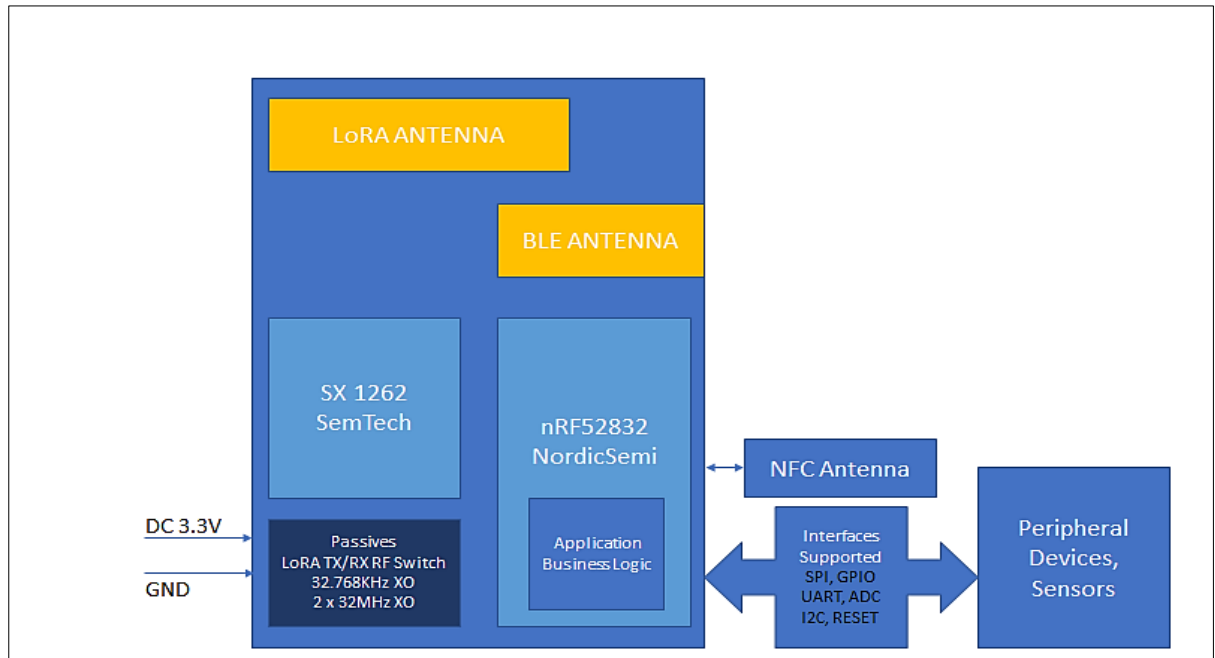
2.4 GHz transceiver	<ul style="list-style-type: none"> • -96 dBm sensitivity in 2.4GHz mode • Supported data rates: 1 Mbps, 2 Mbps 2.4 GHz low energy mode • -20 to +4 dBm TX power, configurable in 4 dB steps • On-chip balun (single-ended RF) • 5.3 mA peak current in TX (0 dBm) • 5.4 mA peak current in RX • RSSI (1 dB resolution)
ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz	<ul style="list-style-type: none"> • 215 EEMBC CoreMark® score running from flash memory • 58 μA/MHz running from flash memory • 51.6 μA/MHz running from RAM • Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace microcell (ITM)

	<ul style="list-style-type: none"> • Serial wire debug (SWD) • Trace port
Flexible power management	<ul style="list-style-type: none"> • 1.7 V–3.6 V supply voltage range • Fully automatic LDO and DC/DC regulator system • Fast wake-up using 64 MHz internal oscillator • 0.3 μA at 3 V in System OFF mode • 0.7 μA at 3 V in System OFF mode with full 64 kB RAM retention • 1.9 μA at 3 V in System ON mode, no RAM retention, wake on RTC
Memory	<ul style="list-style-type: none"> • 512 kB flash/64 kB RAM • 256 kB flash/32 kB RAM
Other wireless features	<ul style="list-style-type: none"> • Microprocessor Control Unit (MCU): nRF52832 • Nordic SoftDevice ready • Support for concurrent multi-protocol • Type 2 near field communication (NFC-A) tag

	<p>with wakeup-on-field and touch-to-pair capabilities</p> <ul style="list-style-type: none"> • 12-bit, 200 kSPS ADC - 8 configurable channels with programmable gain • 64 level Comparator
<p>Other LoRa features</p>	<ul style="list-style-type: none"> • Semtech’s SX1262 SoC solution • LoRa and FSK modem • 170 dB maximum link budget (SX1262/ 68) • +22 dBm or +15 dBm high efficiency PA • Low RX current of 4.6mA • Integrated DC-DC converter and LDO • Programmable bit rate up to 62.5 kbps LoRa and 300 kbps FSK • High sensitivity: down to -148dBm • 88 dB blocking immunity at 1 MHz offset • Co-channel rejection of 19 dB in LoRa mode • FSK, GFSK, MSK, GMSK and LoRa modulation

	<ul style="list-style-type: none">• Built-in bit synchronizer for clock recovery• Automatic Channel Activity Detection (CAD) with ultra-fast AFC
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4. Application Block Diagram



5. Interfaces

5.1. Power Supply

Regulated power supply is required for this module. The input voltage (Vcc) range should be 1.8V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power supply.

5.2. System Function Interfaces

5.2.1. GPIOs

The general purpose I/O is organized as one port with up to 20 I/Os enabling access and control of up to 20 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

- All pins can be configured as PWM
- There are 7 ADC/LPCOMP input in the 20 I/Os

5.2.2. Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps, 250kbps and 400 kbps.

5.2.3. Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4. SPI Bus

The SPI interface is an alternate function of GPIO pins. The module can be a master device (or slave device) that uses terminals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CS is implemented using any spare IO digital output pins to allow multi-dropping. Each multidrop SPI slave device requires a unique and dedicated CS line.

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers to and from multiple slaves. Individual chip select signals are necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double-buffered.

The SPI peripheral supports SPI modes 0, 1, 2, and 3. The module has 1 SPI port available.

5.2.5. UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. It supports the following baud rate in bps unit:

1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

Note: The GPIOs are used for each SPI/TWI/UART interface line and can be chosen from any GPIOs on the device and configured independently.

5.2.6. Analogue to Digital Converter (ADC)

The 12-bit incremental Analogue to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference pre-scaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analogue inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

5.2.7. Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analogue inputs on the device. Additionally, the low power comparator can be used as an analogue wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8. Reset

The reset pin of the module is in the internal pull-high state. When the reset pin of the module is input to a low level, the module will be automatically reset.

5.2.9. NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum. With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed below are the main features for the NFC peripheral:

- NFC-A listen mode operation

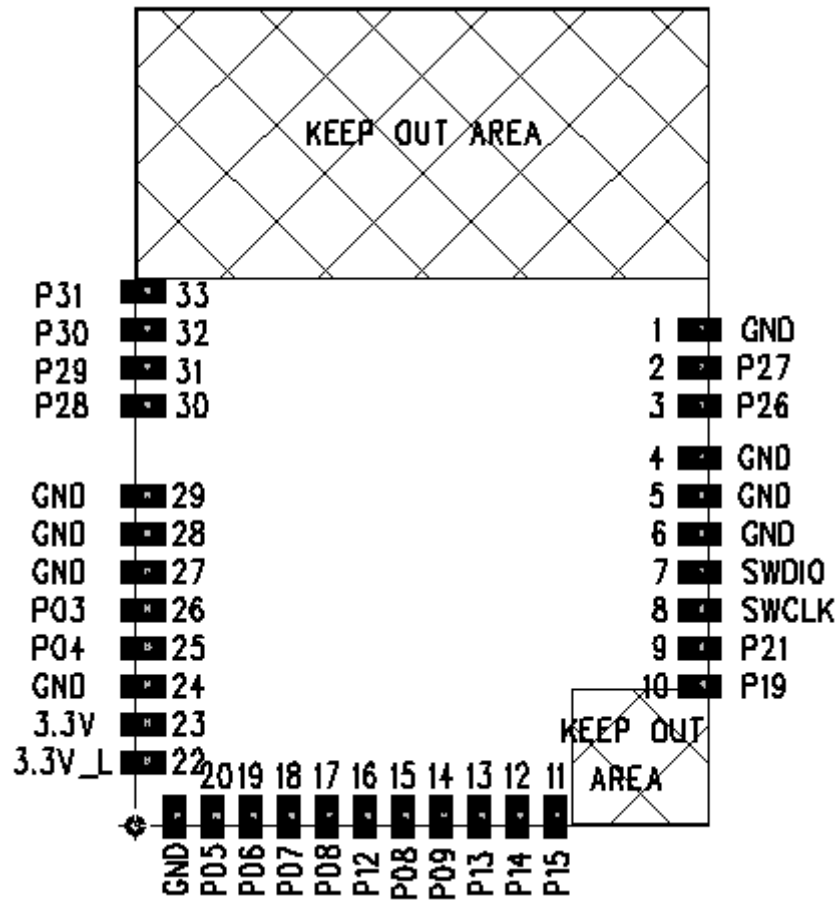
- 13.56 MHz input frequency
- Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frames assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, CRC and parity functions

6. Module Specifications

Hardware Features	
Model	CBTLRM01
LoRa Antenna	NN02-224
RF Antenna	NN02-101
Chipset Solution	Nordic nRF52832 and Semtech SX1262
Voltage	1.8V ~ 3.6V
Dimensions (L x W x H)	21mm x 30mm x 3.4mm
Software/ SDK	CWD Limited has developed an Application Development suite which enables the user to develop their own application logic.
Wireless Features	
Wireless Standards	ANT, 2.4GHz, LoRaWAN™
Frequency Range	2.4GHz ISM band and 150 MHz to 960 MHz bands for LoRa
Data Rates	1Mbps, 2Mbps RF,
Wireless Security	AES HW Encryption
Transmit Power	+4dbm for 2.4GHz and +20dbm for LoRa

7. Module Pin-out and Pin Description

7.1. Module Pin-out

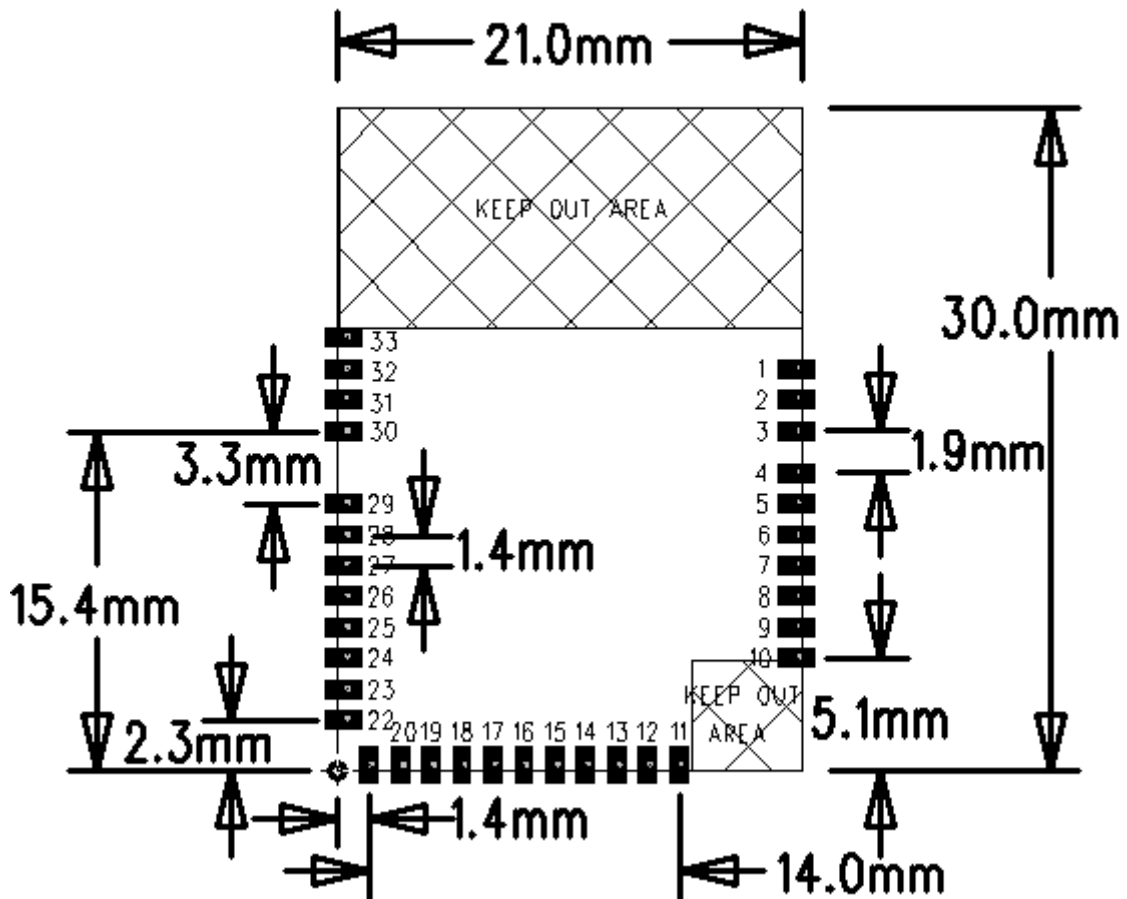


7.2. Pin Description

Pin No.	Pin Name	nRF52832 MCU Pin	Pin Description
1	GND	GND	GND
2	P27	P27/SCL	General purpose I/O pin
3	P26	P26/SDA	General purpose I/O pin
4	GND	GND	GND
5	GND	GND	GND
6	GND	GND	GND
7	SWDIO	SWDIO	Programming Data
8	SWCLK	SWCLK	Programming clock
9	P21	P21/RESET	General purpose I/O pin. Configurable as pin Reset
10	P19	P19	General purpose I/O pin
11	P15	P15	General purpose I/O pin
12	P14	P14	General purpose I/O pin
13	P13	P13	General purpose I/O pin
14	P10	P10/NFC2	General purpose I/O pin/NFC antenna connection
15	P09	P09/NFC1	General purpose I/O pin/NFC antenna connection
16	DIO1	P12	General purpose I/O pin
17	RX	P08/RX	General purpose I/O pin
18	P07	P07	General purpose I/O pin

19	TX	P06/TX	General purpose I/O pin
20	P05	P05	General purpose I/O pin
21	GND	GND	GND
22	3.3V_L	3.3V for LoRa	PWR
23	3.3V	3.3V	PWR
24	GND	GND	GND
25	P04	P04/AIN2	General purpose I/O pin (SAADC/COMP/LPCOMP)
26	P03	P03/AIN1	General purpose I/O pin (SAADC/COMP/LPCOMP)
27	GND	GND	GND
28	GND	GND	GND
29	GND	GND	GND
30	P28	P28	General purpose I/O pin (SAADC/COMP/LPCOMP)
31	P29	P29	General purpose I/O pin (SAADC/COMP/LPCOMP)
32	P30	P30	General purpose I/O pin (SAADC/COMP/LPCOMP)
33	P31	P31	General purpose I/O pin (SAADC/COMP/LPCOMP)

8. PCB Footprint and Dimensions



9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage Temp.	-40	125	°C
ESD Protection		2000	V
Supply Voltage	-0.3	3.9	V
Voltage on I/O Pin	-0.3	3.6	V

9.2. Recommended Operating Range

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temp.	TA	-40		85	°C
Power Supply	VCC	1.8	3.3	3.6	V
Input Low Voltage	VIL	-0.3		0.3*VCC	V
Input High Voltage	VIH	0.7*VCC		VCC	V
Sleep current	Isleep		4		uA
Peak Pulse current	Ic		135		mA

10. Ordering Information

Module No.	Shielding
CBTLRM01	No/YES

11. Contact Information

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