CWD LIMITED

Datasheet

CBTMN33

An advanced multiprotocol RF module

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1. General Description

The module CBTMN33 is a powerful, highly flexible, ultra-low power RF module using Nordic nRF52833 SoC solution developed by CWD Limited. With a 64 MHz Arm® Cortex-M4 with FPU available 512 KB Flash + 128 KB RAM, embedded 2.4GHz multiprotocol transceiver and an integrated PCB trace.

This module incorporates: GPIO, UART, SPI, TWI, PDM HS-SPI, I2S, PWM 12-bit ADC, NFC USB 2.0 GPIO, SPI, UART, I2C, I2S, PMD, PWM, ADC interfaces for connecting peripherals and sensors.

2. Applications

The extended 105°C temperature qualification coupled with a generous amount of memory and dynamic multiprotocol support ensures the CBTMN33 is an ideal device for a wide range of commercial and industrial applications.

A brief of the applications is below:

Advanced wearables	• Health/fitness sensor and monitor devices • Wireless payment enabled devices
Advanced computer peripherals and I/O devices	• Mouse • Keyboard • Multi-touch trackpad
Internet of Things (IoT)	• Smart home sensors and controllers • Industrial IoT sensors and controllers
Interactive entertainment devices	• Remote controls • Gaming controller/HID/VR
Professional lighting	
Asset tracking	
Way finding	
Multiprotocol devices	
Mesh networks	
Toys	

3. Features

IEEE 802.15.4-2006, 2.4 GHz transceiver	• -96 dBm sensitivity in 1 Mbps low power RF mode • -103 dBm sensitivity in 125 kbps low power RF mode (long range) • -20 to +8 dBm TX power, configurable in 4 dB steps • On-air compatible with nRF52, nRF51, nRF24L, and nRF24AP Series • Supported data rates: ▪ Low power RF – 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps ▪ IEEE 802.15.4-2006 – 250 kbps ▪ Proprietary 2.4 GHz – 2 Mbps, 1 Mbps • Angle-of-arrival (AoA) and angle-of-departure (AoD) direction finding • Single-ended antenna output (on-chip balun)

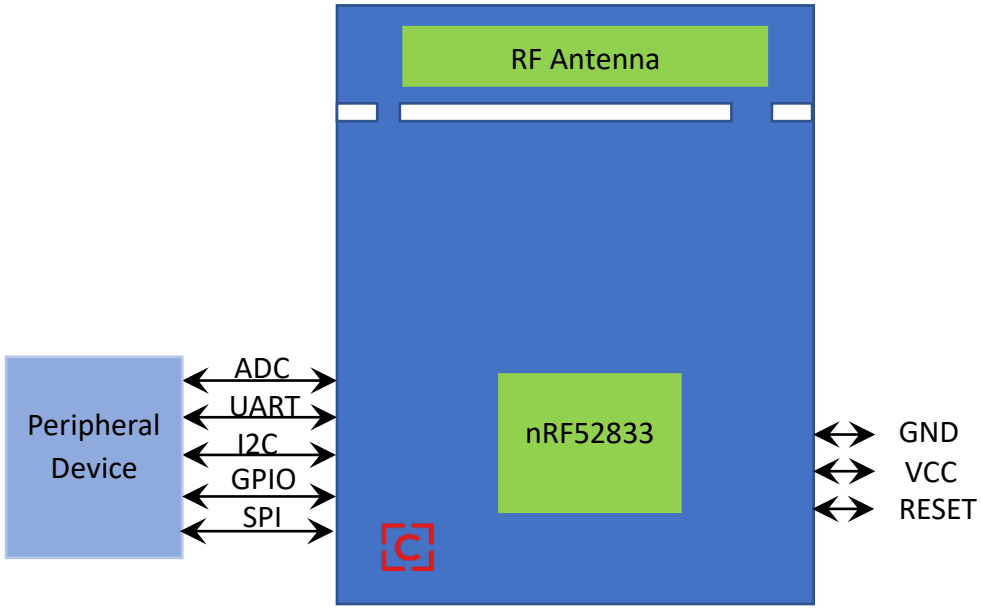
	• 128-bit AES/ECB/CCM/AAR co-processor (on the fly packet encryption) • 4.9 mA peak current in TX (o dBm) • 4.6 mA peak current in RX • RSSI (1 dB resolution)
ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz	• 217 EEMBC CoreMark® score running from flash memory • 52 µA/MHz running CoreMark from flash memory • 38 µA/MHz running CoreMark from RAM • Watchpoint and trace debug modules (DWT, ETM, and ITM) • Serial wire debug (SWD)
Rich set of features	• Secure boot ready • Flash access control list (ACL) • Debug control and configuration • Access port protection (CTRL-AP) • Secure erase
Flexible power management	• 1.7 V–5.5 V supply voltage range

	• On-chip DC/DC and LDO regulators with automated low current modes • Automated peripheral power management • Fast wake-up using 64 MHz internal oscillator • 0.6 µA at 3 V in System OFF mode, no RAM retention • 1.5 µA at 3 V in System ON mode, no RAM retention, wake on RTC
Memory	• 512 kB flash and 128 kB RAM
Advanced on-chip features	• USB 2.0 full speed (12 Mbps) controller • High-speed 32 MHz SPI • Type 2 near field communication (NFC-A) tag with wake-on field • Touch-to-pair support • Programmable peripheral interconnect (PPI) • 40 general purpose I/O pins • EasyDMA automated data transfer between memory and peripherals

Other features	• Microprocessor Control Unit (MCU): nRF52833 • Nordic SoftDevice ready with support for concurrent multiprotocol • 12-bit 200 ksps ADC – 8 configurable channels with programmable gain • 64 level comparator • 15 level low-power comparator with wake-up from System OFF mode • Temperature sensor • 4x four channel pulse width modulator (PWM) unit with EasyDMA • Audio peripherals – I2S, digital microphone interface (PDM) • 5x 32-bit timer with counter mode • Up to 4x SPI master/3x SPI slave with EasyDMA • Up to 2x I2C compatible two-wire master/slave • 2x UART (CTS/RTS) with EasyDMA

	• Quadrature decoder (QDEC) • 3x real-time counter (RTC) • Single crystal operation • Operating temperature from -40 to 105 °C

4. Application Block Diagram



5. Interfaces

5.1. Power Supply

The module needs regulated power supply. The input voltage Vcc range should 1.7V to 5.5V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

5.2. System Function Interfaces

5.2.1. GPIOs

The general purpose I/O is organized as one port with up to 40 I/Os enabling access and control of up to 40 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

- All pins can be individually configured to carry serial interface or quadrature demodulator signals
- All pins can be configured as PWM
- There are 8 ADC/LPCOMP input in the 40 I/Os

5.2.2. Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps, 250kbps and 400 kbps.

5.2.3. Flash Program I/Os

The module has two programmer pins, SWDCLK pin and SWDIO pin respectively. The two-pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4. Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers.

The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line and can be chosen from any GPIOs on the device and configured independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral support SPI mode 0, 1, 2, and 3. The module has 3 SPI ports, and their properties are as below:

Instance	Master / Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

5.2.5. UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. Support the following baud rate in bps unit: 1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

Note: The GPIOs are used for each SPI/TWI/UART interface line and can be chosen from any GPIOs on the device and configured independently.

5.2.6. Analogue to Digital Converter (ADC)

The 12-bit incremental Analogue to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference pre scaling, and sample resolution (8, 10 and 12 bit).

Note: The ADC module uses the same analogue inputs as the LPCOMP module. Only one of the modules can be enabled at a time.

Module Pin Number	NRF PIN Number	Description
7	P0_02/AIN0	General Purpose I/O SAADC/COMP/LPCOMP INPUT
8	P0_31/AIN7	General Purpose I/O SAADC/COMP/LPCOMP INPUT
10	P0_29/AIN5	General Purpose I/O SAADC/COMP/LPCOMP INPUT
11	P0_03/AIN1	General Purpose I/O SAADC/COMP/LPCOMP INPUT
12	P0_30/AIN6	General Purpose I/O SAADC/COMP/LPCOMP INPUT
13	P0_28/AIN4	General Purpose I/O

		SAADC/COMP/LPCOMP INPUT
14	P0_05/AIN3	General Purpose I/O SAADC/COMP/LPCOMP INPUT
16	P0_04/AIN2	General Purpose I/O SAADC/COMP/LPCOMP INPUT

5.2.7. Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analogue inputs on the device. Additionally, the low power comparator can be used as an analogue wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8. Reset

The reset pin of the module is in the internal pull-high state. When the reset pin of the module is input to a low level, the module will be automatically reset. After the reset pin is used, the parameters of the current setting will not be ANT.

5.2.9. NFC

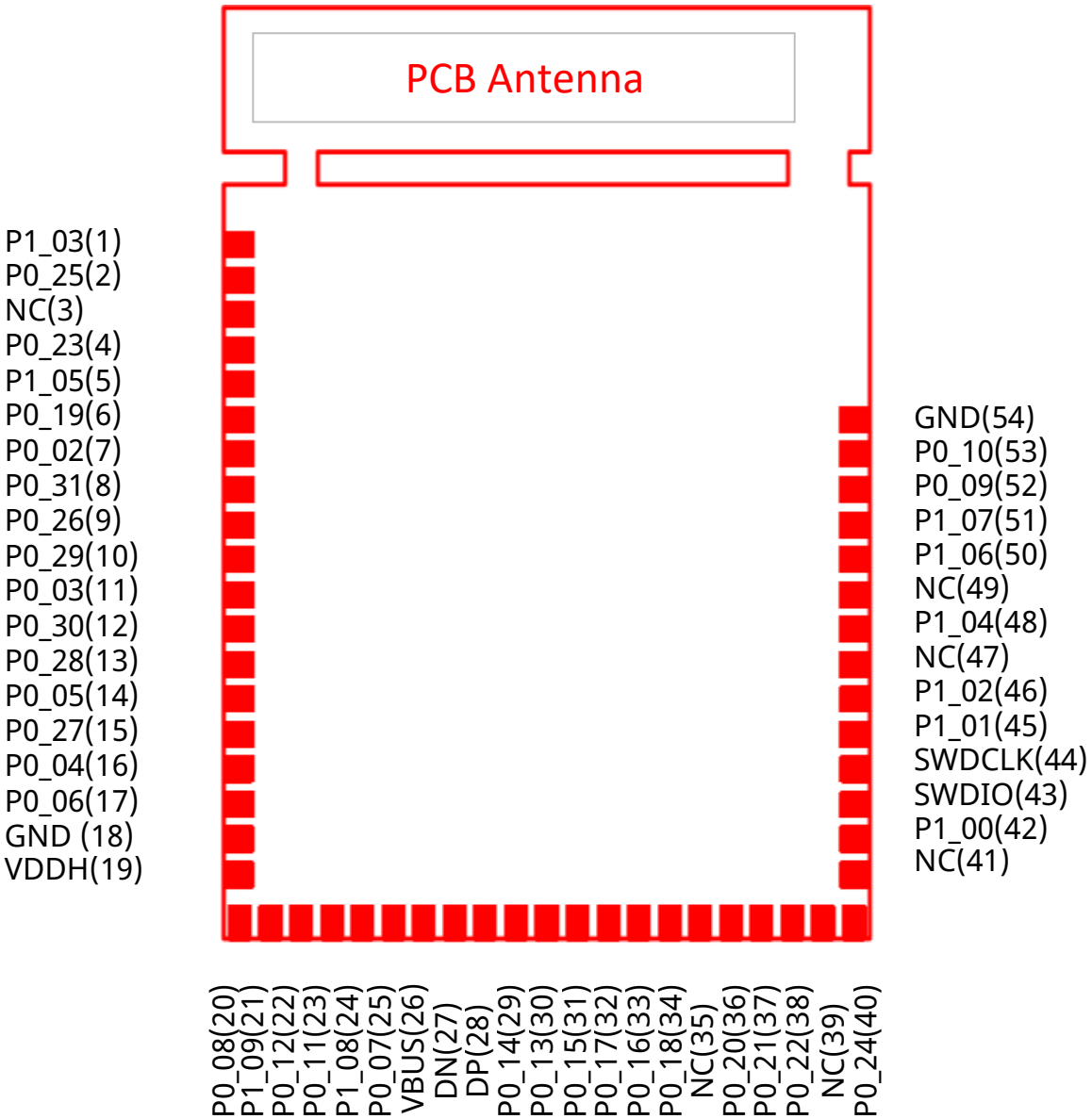
The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum. With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

6. Module Specifications

Hardware Features	
Model	CBTMN33
Antenna Type	PCB Antenna
Chipset Solution	Nordic nRF52833
Voltage	1.7V ~ 5.5V
Temperature	-40°C to +105°C
Dimension (L x W x H)	25.4 x 20.07 x 2.7 mm
Wireless Features	
Wireless Standards	ANT and 2.4GHz proprietary
Frequency Range	2.400GHz to 2.4835GHz
On-air data rate	• Low power RF: 2 Mbps/1 Mbps • 2.4 GHz proprietary: 2 Mbps/1 Mbps
Wireless Security	128-bit AES
TX power	Programmable from +8 dBm to -20 dBm in 4 dB steps
RX sensitivity	-89 dBm at 2 Mbps

7. Module Pin-out and Pin Description

7.1. Module Pin-out



7.2. Pin Description

Pin No.	Name	nRF52833 Pin	Pin Function	Description
1	P1_03	B15	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
2	P0_25	A20	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
3	NC	NC	NC	Not connected
4	P0_23	B17	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
5	P1_05	A16	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
6	P0_19	A14	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
7	P0_02	A12	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN0		Analogue Input	Analogue Input

8	P0_31	A8	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN7		Analogue Input	Analogue Input
9	P0_26	G1	Digital I/O	General-Purpose I/O
10	P0_29	A10	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN5		Analogue Input	Analogue Input
11	P0_03	B13	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN1		Analogue Input	Analogue Input
12	P0_30	B9	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN6		Analogue Input	Analogue Input
13	P0_28	B11	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN4		Analogue Input	Analogue Input

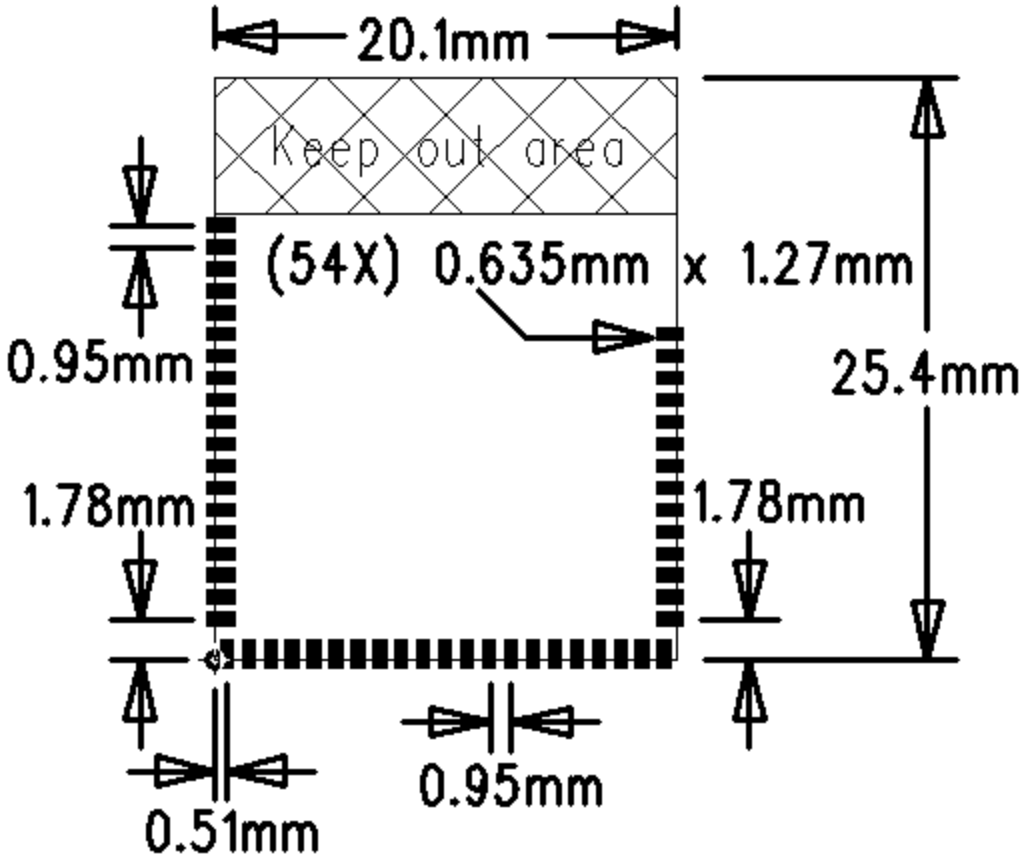
14	P0_05	K2	Digital I/O	General-Purpose I/O
	AIN3		Analogue Input	Analogue Input
15	P0_27	H2	Digital I/O	General-Purpose I/O
16	P0_04	J1	Digital I/O	General-Purpose I/O
	AIN2		Analogue Input	Analogue Input
17	P0_06	L1	Digital I/O	General-Purpose I/O
18	GND		Power	Ground
19	VDDH	Y2	Power	Power supply
20	P0_08	P2	Digital I/O	General-Purpose I/O
21	P1_09	R1	Digital I/O	General-Purpose I/O
	TRACEDATA 3		Trace data	Trace buffer TRACEDATA [3]
22	P0_12	U1	Digital I/O	General-Purpose I/O
	TRACEDATA 1		Trace data	Trace buffer TRACEDATA [1]
23	P0_11	T2	Digital I/O	General-Purpose I/O
	TRACEDATA 2		Trace data	Trace buffer TRACEDATA [2]
24	P1_08	P2	Digital I/O	General-Purpose I/O
25	P0_07	M2	Digital I/O	General-Purpose I/O
	TRACECLK		Trace clock	Trace buffer clock
26	VBUS	AD2	Power	5V input for USB 3.3V regulator
27	DN	AD4	Digital I/O	USB D-

28	DP	AD6	Digital I/O	USB D+
29	P0_14	AC9	Digital I/O	General-Purpose I/O
30	P0_13	AD8	Digital I/O	General-Purpose I/O
31	P0_15	AD10	Digital I/O	General-Purpose I/O
32	P0_17	AD12	Digital I/O	General-Purpose I/O
33	P0_16	AC11	Digital I/O	General-Purpose I/O
34	P0_18	AC13	Digital I/O	General-Purpose I/O (Recommended usage: QSPI / CSN)
	nRESET		Analogue Input	Configurable as system RESET
35	NC	NC	NC	Not connected
36	P0_20	AD16	Digital I/O	General-Purpose I/O
37	P0_21	AC17	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)
38	P0_22	AD18	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)
39	NC	NC	NC	Not connected
40	P0_24	AD20	Digital I/O	General-Purpose I/O
41	NC		NC	Not connected
42	P1_00	AD22	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)

	TRACEDATA 0		Trace data	Trace buffer TRACEDATA [0]
43	SWDIO	AC24	Debug	Debug serial data
44	SWDCLK	AA24	Debug	Serial wire debug clock input for debug and programming
45	P1_01	Y23	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
46	P1_02	W24	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
47	NC	NC	NC	Not connected
48	P1_04	U24	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
49	NC	NC	NC	Not connected
50	P1_06	R24	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
51	P1_07	P23	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
52	P0_09	L24	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	NFC1		NFC input	NFC antenna connection

53	P0_10	J24	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	NFC2		NFC input	NFC antenna connection
54	GND		Power	Ground

8. PCB Footprint and Dimensions



Dimension: (L)25.4mm x (W)20.07mm x (H)2.7mm (+-5%)

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage Temp	-40	125	°C
ESD Protection		4000	V
Supply Voltage	-0.3	5.8	V
Voltage on I/O PIN	-0.3	3.9	V

9.2. Recommended Operator Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	TA	-40		105	°C
Power Supply	VCC	2.5	3.7	5.5	V
Input Low Voltage	VIL	-0.3		0.3xVCC	V
Input High Voltage	VIH	0.7xVCC		VCC	V

10. Contact Information

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