CWD LIMITED

Datasheet

CBTMN40

An advanced multiprotocol ultra-low power RF module

Table of Contents

1. Revision History

Version	Date	Description	Approver
1.00	02 Apr 2018	Initial Release	SXA
1.01	10 Apr 2018	Revised Product Dimensions	SXA
1.02	15 Apr 2018	Added Shielding Information	SXA
1.03	14 May 2018	Added DC-DC Convertor	SXA

Table 1: Revision History

2. Abbreviations

Abbreviations	Description
RF	Radio frequency
TX	Transmission
RX	Reception
FPU	Floating Point Unit
RSSI	Received Signal Strength Indication
AES	Advanced Encryption Standard
ECB	Electronic Codebook Mode Encryption
CCM	Cipher Block Chaining-Message Authentication Code
PWM	Pulse Width Modulation
AAR	Accelerated Address Resolver
DMA	Direct Memory Access
CTS	Clear to Send
RTS	Request to Send
PLL	Phase Locked Loop
GPIO	General Purpose Input Output
QSPI	Quad Serial Peripheral Interface
SPI	Serial Peripheral Interface
ADC	Analogue to Digital Convertor
NFC	Near Field Communication

Table 2: Acronym Description Table

3. General Description

The CBTMN40 is a powerful, highly flexible, ultra-low power RF module using Nordic nRF52840 SoC solution developed by CWD Limited. With an ARM Cortex M4F MCU available 1MB Flash, 256KB RAM, embedded 2.4GHz multiprotocol transceiver and an integrated PCB trace antenna or x.FL connector for external antenna.

The module incorporates: GPIO, SPI, UART, I2C, I2S, PMD, PWM, ADC, NFC, and USB interfaces for connecting peripherals and sensors.

4. Features

IEEE 802.15.4, 2.4 GHz transceiver	• -95 dBm sensitivity in 1 Mbps low power RF mode • -103 dBm sensitivity in 125 kbps low power RF mode (long range) • +8 dBm TX power (down to -20 dBm in 4 dB steps) • On-air compatible with nRF52, nRF51, nRF24L, and nRF24AP Series • RSSI (1 dB resolution) • 4.8 mA peak current in TX (0 dBm) • 4.8 mA peak current in TX (0 dBm) • Supported data rates: ▪ Low power RF – 2 Mbps, 1 Mbpss, 500 kbps, and 125 kbps ▪ IEEE 802.15.4-2006 – 250 kbps ▪ Proprietary 2.4 GHz – 2 Mbps, 1 Mbps

ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz	• 212 EEMBC CoreMark score running from flash memory • 52 µA/MHz running CoreMark from flash memory • Watchpoint and trace debug modules (DWT, ETM, and ITM) • Serial wire debug (SWD)
Flexible power management	• Supply voltage range 1.7V to 3.3V • On-chip LDO regulators with automated low current modes • Regulated supply for external components from 1.8V to 3.3V • Automated peripheral power management • Fast wake-up using 64 MHz internal oscillator • 0.4 µA at 3 V in System OFF mode, no RAM retention • 1.5 µA at 3 V in System ON mode, no RAM retention, wake on RTC
Memory	• 1 MB flash and 256 kB RAM
HW accelerated security	• ARM Trust Zone Cryptocell 310 security subsystem

	• 128-bit AES/ECB/CCM/AAR co-processor (on the fly packet encryption)
Advanced on-chip features	• USB 2.0 full speed (12 Mbps) controller • QSPI 32 MHz interface • High-speed 32 MHz SPI • Type 2 near field communication (NFC-A) tag with wake-on field • Programmable peripheral interconnect (PPI) • 46 general purpose I/O pins • EasyDMA automated data transfer between memory and peripherals
Other features	• 12-bit, 200ksps ADC – 8 configurable channels with programmable gain • 4 x 4 channel pulse width modulator (PWM) units with EasyDMA • Audio peripherals: I2S, digital microphone interface (PDM) • 5 X 32-bit timers with counter mode

	• Up to 4xSPI masters/3xSPI slaves with EasyDMA • Up to 2xI2C compatible 2-wire masters/slaves • 2xUART (CTS/RTS) with EasyDMA • Quadrature decoder (QDEC) • 3x24-bit real-time counters (RTC)

5. Applications

Due to varied support of protocols and stacks, CBTMN40 can support varied applications. A brief of the applications is as below:

Internet of Things	• Smart home products • Industrial mesh networks • Smart city infrastructure
Advanced wearables	• Connected watches • Advanced personal fitness devices • Wearables with wireless payment • Connected health • Virtual/Augmented reality applications
Interactive entertainment devices	• Advanced remote controls • Gaming controller
Personal area networks	• Health/Fitness sensor and monitor device • Medical device

6. Application Block Diagram

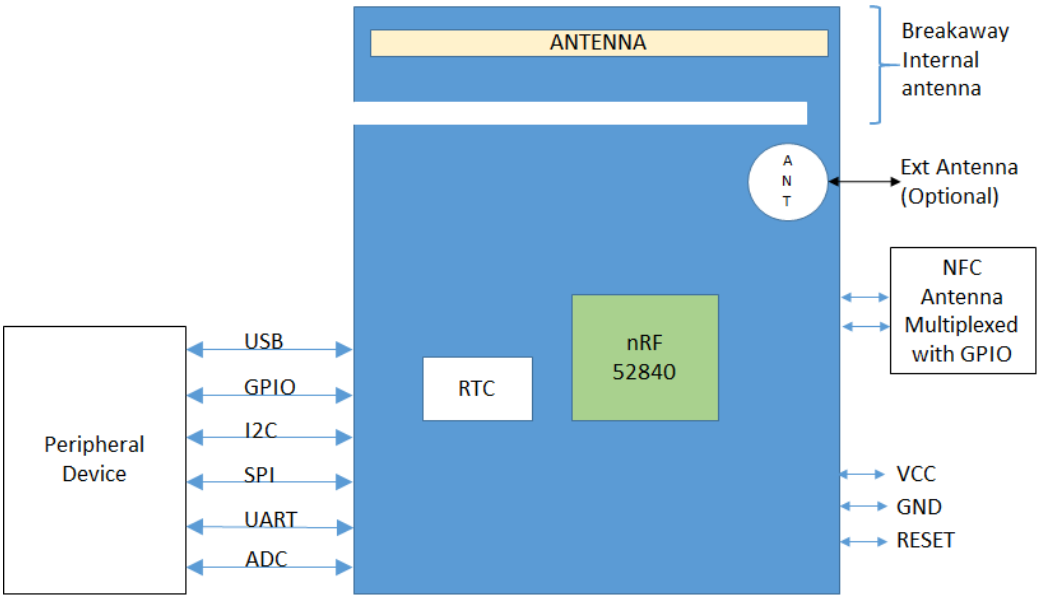

Fig. 1: Block Diagram of Module

7. PCB Dimensions and Pin Indication

PCB Size: (L) 25.4mm x (W) 20.07mm

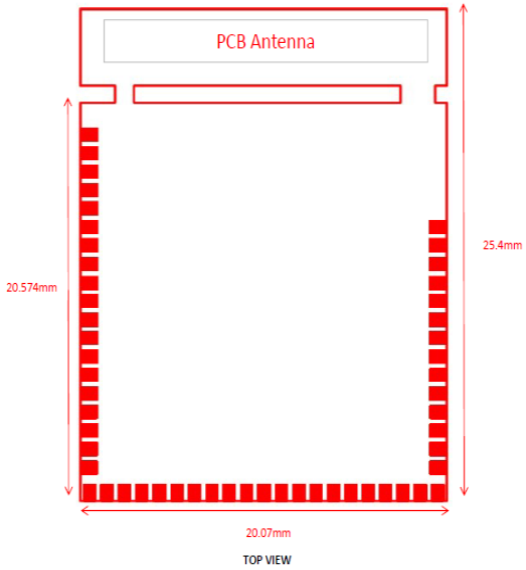

Fig. 2: PCB Dimension

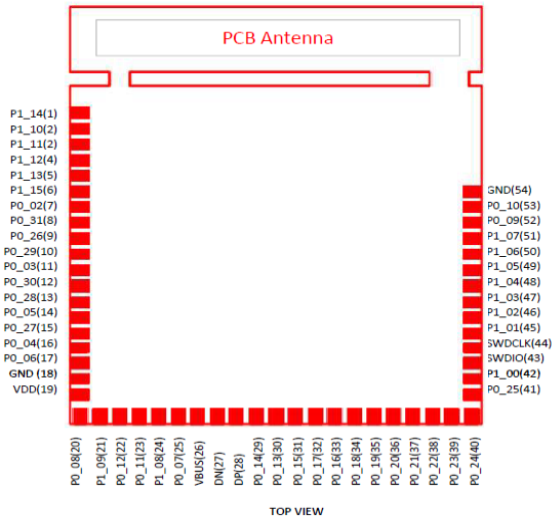

Fig. 3: PCB Pin Indication

8. PCB Footprint

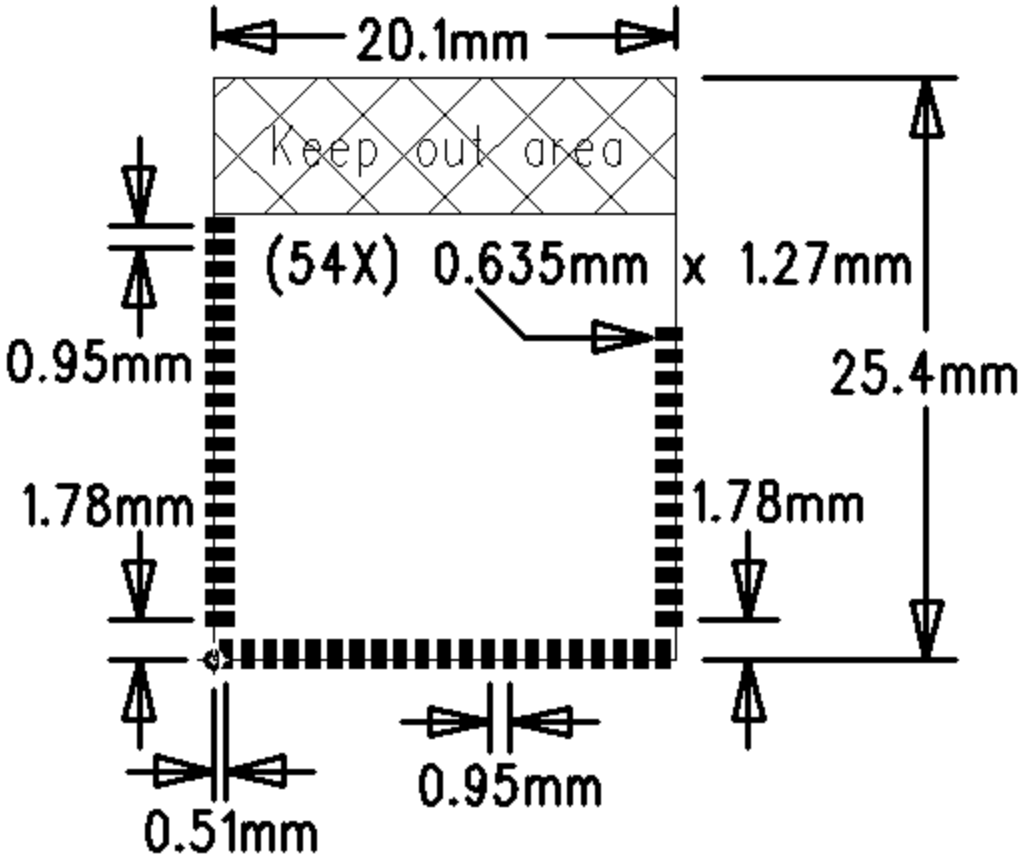

Fig. 4: PCB Footprint

9. Pin Assignment

Pin No.	Name	Pin Function	Description
1	P1_14	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
2	P1_10	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
3	P1_11	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
4	P1_12	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
5	P1_13	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
6	P1_15	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
7	P0_02	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN0	Analogue Input	Analogue Input
8	P0_31	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN7	Analogue Input	Analogue Input
9	P0_26	Digital I/O	General-Purpose I/O

10	P0_29	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN5	Analogue Input	Analogue Input
11	P0_03	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN1	Analogue Input	Analogue Input
12	P0_30	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN6	Analogue Input	Analogue Input
13	P0_28	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	AIN4	Analogue Input	Analogue Input
14	P0_05	Digital I/O	General-Purpose I/O
	AIN3	Analogue Input	Analogue Input
15	P0_27	Digital I/O	General-Purpose I/O
16	P0_04	Digital I/O	General-Purpose I/O
	AIN2	Analogue Input	Analogue Input
17	P0_06	Digital I/O	General-Purpose I/O
18	GND	Power	Ground
19	VDD	Power	Power supply

20	P0_08	Digital I/O	General-Purpose I/O
21	P1_09	Digital I/O	General-Purpose I/O
	TRACEDATA3	Trace data	Trace buffer TRACEDATA [3]
22	P0_12	Digital I/O	General-Purpose I/O
	TRACEDATA1	Trace data	Trace buffer TRACEDATA [1]
23	P0_11	Digital I/O	General-Purpose I/O
	TRACEDATA2	Trace data	Trace buffer TRACEDATA [2]
24	P1_08	Digital I/O	General-Purpose I/O
25	P0_07	Digital I/O	General-Purpose I/O
	TRACECLK	Trace clock	Trace buffer clock
26	VBUS	Power	5V input for USB 3.3V regulator
27	DN	Digital I/O	USB D-
28	DP	Digital I/O	USB D+
29	P0_14	Digital I/O	General-Purpose I/O
30	P0_13	Digital I/O	General-Purpose I/O
31	P0_15	Digital I/O	General-Purpose I/O
32	P0_17	Digital I/O	General-Purpose I/O
33	P0_16	Digital I/O	General-Purpose I/O
34	P0_18	Digital I/O	General-Purpose I/O
			(Recommended usage: QSPI / CSN)
	nRESET	Analogue Input	Configurable as system RESET

35	P0_19	Digital I/O	General-Purpose I/O (Recommended usage: (QSPI / SCK)
36	P0_20	Digital I/O	General-Purpose I/O
37	P0_21	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)
38	P0_22	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)
39	P0_23	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)
40	P0_24	Digital I/O	General-Purpose I/O
41	P0_25	Digital I/O	General-Purpose I/O
42	P1_00	Digital I/O	General-Purpose I/O (Recommended usage: QSPI)
	TRACEDATA0	Trace data	Trace buffer TRACEDATA [0]
43	SWDIO	Debug	Debug serial data
44	SWDCLK	Debug	Serial wire debug clock input for debug and programming
45	P1_01	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
46	P1_02	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
47	P1_03	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
48	P1_04	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)

49	P1_05	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
50	P1_06	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
51	P1_07	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
52	P0_09	Digital I/O	General-Purpose I/O
53	P0_10	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	NFC2	NFC input	NFC antenna connection
54	GND	Power	Ground
53	P0_10	Digital I/O	General-Purpose I/O (Standard drive, low frequency I/O only)
	NFC2	NFC input	NFC antenna connection
54	GND	Power	Ground

Table 3: Pin Assignment

10. Interfaces

10.1. Power Supply

Regulated power for the SKB369 is required. The input voltage Vcc range should be 1.7V to 3.3V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

10.2. System Function Interfaces

10.2.1. GPIOs

The general purpose I/O is organized as one port with up to 46 I/Os enabling access and control of up to 46 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

- All pins can be individually configured to carry serial interface or quadrature demodulator signals
- All pins can be configured as PWM
- There are 6 ADC/LPCOMP input in the 46 I/Os

10.2.2. Two-wire Interface

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching and supporting data rates of 100 kbps, 250kbps and 400 kbps.

10.2.3. Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

10.2.4. Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

Control of chip select signals is left to the application through use of GPIO signals.

SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line and can be chosen from any GPIOs on the device and configured independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI mode 0, 1, 2, and 3. The module has 3 SPI ports and their properties are as below:

Instance	Master / Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

Table 4: SPI Port Description

10.2.5. UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. Support the following baud rate in bps unit: 1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

Note: The GPIOs are used for each SPI/TWI/UART interface line and can be chosen from any GPIOs on the device and configured independently.

10.2.6. Analogue to Digital Converter

The 12-bit incremental Analogue to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference pre-scaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analogue inputs as the LPCOMP module. Only one of the modules can be enabled at a time.

Module PIN Number	nRF52840 PIN Number	Description
7	P0.02/AIN0	General Purpose I/O SAADC/COMP/LPCOMP input
11	P0.03/AIN1	General Purpose I/O SAADC/COMP/LPCOMP input
16	P0.04/AIN2	General Purpose I/O SAADC/COMP/LPCOMP input
14	P0.05/AIN3	General Purpose I/O SAADC/COMP/LPCOMP input
13	P0.28/AIN4	General Purpose I/O SAADC/COMP/LPCOMP input

10	P0.29/AIN5	General Purpose I/O SAADC/COMP/LPCOMP input
12	P0.30/AIN6	General Purpose I/O SAADC/COMP/LPCOMP input
08	P0.31/AIN7	General Purpose I/O SAADC/COMP/LPCOMP input

10.2.7. Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analogue inputs on the device. Additionally, the low power comparator can be used as an analogue wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

10.2.8. Reset

The reset pin of the module is in the internal pull-high state. When the reset pin of the module is input to a low level, the module will be automatically reset. After the reset pin is used, the parameters of the current setting will not be ANT.

10.2.9. NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum. With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

11. Main Chip Solution

RF IC	Crystal Frequency
Nordic nRF52840	32 Mhz and 32.768 Khz

12. Electrical Characteristics

12.1. Absolute Maximum Ratings

Parameter	Condition	Min.	Typical	Max.	Unit
Storage Temperature		-40		125	°C
ESD Protection	VESD			2000	V
Supply Voltage	VCC, VBus	-0.3		3.9	V
Voltage on Any I/O Pin		-0.3		3.63	V

Table 5: Maximum Ratings

12.2. Recommended Operating Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	TA	-40	25	85	°C

Power Supply	VCC	1.7	3.3	3.6	V
Input Low Voltage	VIL	0		0.3xVC	V
Input High Voltage	VIH	0.7xVC		VCC	V

Table 6: Operating Condition

12.3. Current Ratings

System State	TX Peak @ 4dBm	RX Peak	Sleep Mode (Average)	Idle Mode (Average)
Current (peak) @ 3V	7.5mA	5.4 mA	4 uA	4 uA

Table 7: Current Ratings

13. Contact Information

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