C CWD LIMITED

Datasheet CNBMM01

NB-IoT R14 solution, 3GPP R13 (NB1) and R14 (NB2) standards



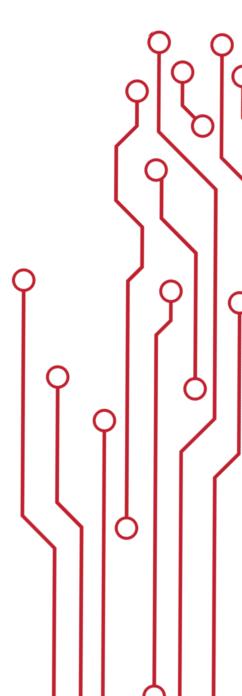




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1. General Description

The module CNBMM01 supports a full frequency band from 450MHz to 2.1GHz of 3GPP R13 (NB1) and R14 (NB2) standards for a wide range of IoT applications including smart home control, logistics tracking and smart meters.

The NB module is based on MediaTek's chipset MT2625 which combines an ARM® Cortex® – M microcontroller (MCU), pseudo-static RAM (PSRAM), flash memory and power management unit (PMU) into a small package to lower the cost of production while also speeding up time-to-market. The module's advanced power consumption technology enables IoT devices to work with chargeable batteries for years.

2. Applications

Due to varied support of protocols and stacks, the CNBMM01 module can support various applications. A brief of the applications is as below:

- Sensor networks
- Logistics and asset tracking
- Smart energy
- Smart building automation
- Smart agriculture
- Industrial
- Retail and monitor devices
- Medical devices
- Smart wearables
- Smart parking
- Home automation
- Cloud beacons
- Smart metering
- Static or mobile IoT implementations



3. Features

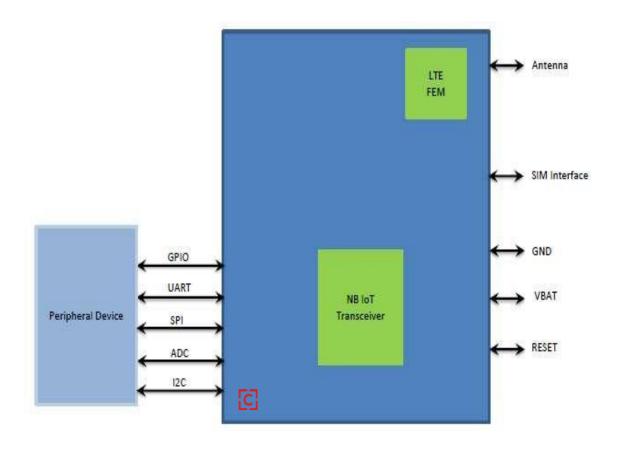
	-
	Compliant with 3GPP R13/R14 NB-IoT
	standard
	Supports DL 200KHz bandwidth/UL
	single tone and multi-tone
NB-IoT transceiver	Supported RF bands:
	B1/B2/B3/B4/B5/B8/B11/B12/B13/B14/
	B17/B18/B19/B20/B21/B25/B26/B28/B31/
	B66/B70/B71/B72/B74/B85
	Supports PSM and eDRX mode
	• 156MHz ARM® Cortex® - M4 with FPU
	and MPU
	MCU operating frequency at
	26/78/104MHz
	• 14 DMA channels
	One RTC timer, one 64-bit and five 32-bit
Microcontroller	general purpose timers
subsystem	Development support: SWD, JTAG
	Crypto engine
	 AES 128/192/256 bits
	■ DES, 3DES
	■ MD5, SHA-1/224/256/384/512
	True random number generator
	JTAG password protection
Memory	Up to 32KB SYSRAM, with zero-wait state

	and 52MHz maximum frequency
	• Up to 32KB L1 cache, with high hit rate,
	zero- wait state and 104MHz maximum
	frequency
	Embedded 32Mbits flash
	■ Sleep current 200nA
	Maximum frequency 78MHz
	Embedded 32Mbits pseudo-SRAM
	■ Sleep current 10uA
	Maximum frequency 78MHz
	Two SDIO 2.0 masters and one SDIO 2.0
	slave
	I2C (3.4Mbps) interfaces
	UART interfaces (3Mbps, UART1/2 with
	hardware flow control)
	Two SPI masters and one SPI slave
	Two I2S interfaces
Communication interfaces	 One 16/24-bit, master/slave mode;
Communication interfaces	One 16-bit, master/slave mode
	with TDM
	■ Both support 16/24/48/96/192kHz
	& 11.025kHz, 22.05kHz, 44.1kHz,
	TX/RX, 2 channels
	Four PWM channels
	GPIOs (5V-tolerant)
	IOs for BPI and MIPI interfaces

	IOs for SIM
	• 5 channel 10-bit AUXADC (PinMux with
	GPIO), maximum input voltage 1.4V
	Three integrated high efficiency buck
	converters with low quiescent current
Power management unit	Four integrated LDO regulators for RTC,
	SIM, RF frontend and GPIOs
	Contains under voltage lockout (UVLO)
	circuit and a reference band gap circuit
	26MHz crystal oscillator
Clock source	32kHz crystal oscillator or internal 32kHz
	RC for RTC



4. Application Block Diagram





5. Interfaces

5.1. Power Supply

Regulated power supply is required for this module. The input voltage (Vcc) range should be 2.1V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

5.2. System Function Interfaces

5.2.1. **GPIOs**

The general purpose I/O is organized as one port with up to 16 I/Os enabling access and control of up to 16 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals



5.2.2. Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of standard mode (100 kbps), fast mode (400kbps) and high-speed mode (3.4mbps).

5.2.3. SWD

Development supports using SWD interface.

5.2.4. Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals.

SPI Master has double-buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line and can be chosen from any GPIOs on the device and configured independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.



The SPI peripheral supports SPI modes 0, 1, 2, and 3. The module has 3 SPI ports, and their properties are as below:

Instance	Master/Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

5.2.5. **UARTs**

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control. UART has both M16C450 and M16550A modes of operation compatible with a range of standard software drivers.

UARTs support baud rate from 110bps up to 3mbps and baud rate auto detection function. UART1 provides hardware and software flow control of the RTS/CTS signals. UARTs can configure data transfer lengths from 5 to 8 bits, with an optimal parity bit and one or two stop bits by software.

5.2.6. Analogue to Digital Converter (ADC)

Analogue multiplexer selects signal from one of the auxiliary input pins. Real world messages such as temperature are monitored and translated to the voltage domain. It converts the multiplexed input signal to 10-bit digital data.



5.2.7. PWRKEY

Long press shutdown is default feature to provide a reliable hardware reset to force shutdown PMU without removing the battery, which detects negative pulse width on PWRKEY. When negative pulse width is greater than the timer setting, the PMU will force shutdown to OFF mode.

There are four types of long press shutdown key pressed timing select timer options: 5s, 8s (default), 11s, 25s.

Note: The timing variation is +/-50% for this feature.

5.2.8. SYSRSTB Cold Reset Application

SYSRSTB is used to reset the PMU when system hangs. This function is default ON by hardware. Cold reset function can be triggered by pressing SYSRSTB for over 32ms de-bounce time. When cold reset is triggered, the system is shut down immediately with immediate off sequence. The shutdown time is 20ms to make sure analogue circuits discharge completely. Then the PMU will do the normal power on.



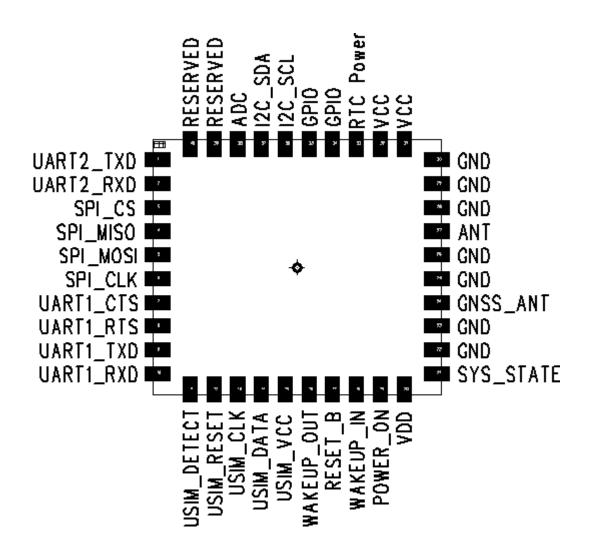
6. Module Specifications

Hardware Features					
Model	CNBMM01				
Antenna Type	External antenna				
Chipset Solution	MT2625				
Voltage	2.1V ~ 3.6V				
Dimensions (L x W x H)	15mm x 17mm x TBDmm				
Wireless and Network Fe	atures				
Wireless Standards	3GPP R13/R14 NB-IoT standard				
Frequency Range	450MHz to 2.1GHz				
Frequency Bands	B1/B2/B3/B4/B5/B8/B11/B12/B13/B14/B17/B18/B 19/B20/B21/B25/B26/B28/B31/B66/B70/B71/B72/ B74/B85				
Protocol Support	UDP, TCP, LWM2M, MQTT-SN, CoAP, Non-IP, IPv4, IPv4v6, IPv6				
Security Feature					
Crypto Engine	AES 128/192/256; CB/CBC; DES/3DES: MD5/ SHA-1/224/256/384/512				



7. Module Pin-out and Pin Description

7.1. Module Pin-out



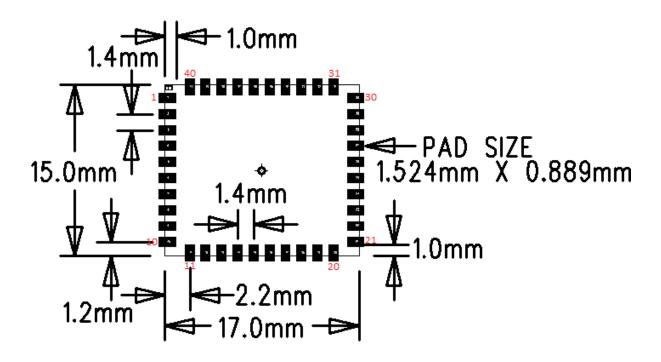
7.2. Pin Description

Pin No.	Pin Name	MTK2625 MCU Pin	Pin Description	
1	UART2_TXD	GPIO5	General purpose I/O pin	
2	UART2_RXD	GPIO2	General purpose I/O pin	
3	SPI_CS	GPIO12	General purpose I/O pin	
4	SPI_MISO	GPIO14	General purpose I/O pin	
5	SPI_MOSI	GPIO13	General purpose I/O pin	
6	SPI_CLK	GPIO15	General purpose I/O pin	
7	UART1_CTS	GPIO18	General purpose I/O pin	
8	UART1_RTS	GPIO23	General purpose I/O pin	
9	UART1_TXD	GPIO17	General purpose I/O pin	
10	UART1_RXD	GPIO16	General purpose I/O pin	
11	USIM_DETECT	GPIO35	General purpose I/O pin	
12	USIM_RESET	SIM0_SRST	SIM card reset	
13	USIM_CLK	SIM0_SCLK	SIM card clock	
14	USIM_DATA	SIM0_SIO	SIM card IO	
15	USIM_VCC	VSIM	SIM card power	
16	WAKEUP_OUT	GPIO27	General purpose I/O pin	
17	RESET_B	PMU_SYSRSTB	System RSTB pin	
18	WAKEUP_IN	RTC_EINT	Dedicate EINT input in RTC	
19	POWER_ON	PMU_PWRKEY	Power key	
20	VDD	DVDD18_MLD O	Power input of SF/EMI group	
21	SYS_STATE	GPIO26	General purpose I/O pin	
22	GND	GND	GND	
23	GND	GND	GND	
24	GNSS_ANT		NC	
25	GND	GND	GND	
26	GND	GND	GND	
27	ANT	ANT	Antenna pin	
28	GND	GND	GND	

29	GND	GND	GND	
30	GND	GND	GND	
31	VCC	VBAT	POWER	
32	VCC	VBAT	POWER	
33	RTC Power		NC	
34	GPIO	GPIO9	General purpose I/O pin	
35	GPIO	GPIO10	General purpose I/O pin	
36	I2C_SCL	GPIO6	General purpose I/O pin	
37	I2C_SDA	GPIO7	General purpose I/O pin	
38	ADC	GPIO30	General purpose I/O pin	
39	RESERVED		NC	
40	RESERVED	FSOURCE_P	eFuse power source	



8. PCB Footprint and Dimensions



Dimensions: 15mm x 17mm x TBDmm

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Parameter	Condition	Min.	Typical	Max.	Unit
Storage Temp.		-40		125	°C
Supply Voltage		-0.3		3.63	V
Voltage on I/O Pin		-0.3		3.63	V

9.2. Recommended Operating Range

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temp.	TA	-40		85	°C
Power Supply	VCC	2.1	3.3	3.6	V
Input Low Voltage	VIL	-0.3		0.15*VCC	V
Input High Voltage	VIH	0.85*VCC		VCC	V



10. Contact Information

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